EEE 3310 Digital Electronics | Fall 2022

# Design Project 2

**Design & Simulation of Digital Circuits with CAD Tools**

Total Points: 150

# Due: 7 December 2022

***Design, simulate, and analyze the following logic gates using HSPICE***. Use the 45-nm CMOS High Performance Predictive Technolog Model. Supply voltage, VDD, should be 1V for all the designs.

1. 2-input NAND gate
2. 2-input NOR gate
3. 2-input XNOR gate

Note: you will need to perform **transient analysis** for this. Apply a pulse at the input (VI). Use the following pulse as input: PULSE (0 1 0n 0.01n 0.01n 4n 8n). Use .**measure** to

measure the tPLH and tPHL values.

|  |  |
| --- | --- |
| **Performance Parameters** | **Basic CMOS Inverter** |
|  |  |
|  |  |
|  |  |

# Part 1: 2-input NAND gate design, simulation, and analysis (40 points)

1. **Determine the widths (W) of all the transistors** in the design such that the delays are almost same as that of the basic inverter in **Part 0**.

# Include the diagram of the 2-input CMOS NAND logic clearly indicating the (W/L) of each transistor. Note: the diagram should NOT be hand-drawn.

# Diagram, schematic Description automatically generated

2n=4,

p=3,

2n=4,

p=3,

1. Model the circuit in HSPICE, perform the HSPICE simulation, and note down the following parameters.

Note: you will need to perform **transient analysis** for this. Apply two pulses at the inputs A and

B. One pulse should have a time period of 8ns, whereas the other should have a period of 16ns. Use .**measure** to measure the values based on the transient response.

|  |  |  |
| --- | --- | --- |
| **Performance Parameters** | **2-input NAND gate** | |
|  | 17.8, 17.3, 9.66 | 14.92ps |
|  | 14.7, 15.4, 16.7 | 15.6ps |
|  | 15.26ps | |
| **Static Power** | 25.9575nW | |
| **Average Power** | 218.407nW | |

**Include the screenshot of the transient response waveform** to observe the inverter operation up to 20ns and the SPICE netist (.sp file).

1. Is the average propagation delay, ,exactly same as that of the basic CMOS inverter from **Part 0**? If not, what is the percentage deviation from the basic inverter’s avergae propagation delay?

# Part 2: 2-input NOR gate design, simulation, and analysis (40 points)

1. **Determine the widths (W) of all the transistors** in the design such that the delays are almost same as that of the basic inverter in **Part 0**.

# Include the diagram of the 2-input CMOS NOR logic clearly indicating the (W/L) of each transistor. Note: the diagram should NOT be hand-drawn.

# Diagram, schematic Description automatically generated

n=2,

n=2,

2p=6,

2p=6,

1. Model the circuit in HSPICE, perform the HSPICE simulation, and note down the following parameters.

|  |  |  |
| --- | --- | --- |
| **Performance Parameters** | **2-input NOR gate** | |
|  | 16.8, 15.6, 17.7 | 16.433ps |
|  | 20.4, 10.4, 18.5 | 16.7ps |
|  | 16.566ps | |
| **Static Power** | 4.1915nW | |
| **Average Power** | 89.04nW | |

**Include the screenshot of the transient response waveform** to observe the inverter operation up to 20ns and the SPICE netist (.sp file).

1. Is the average propagation delay,𝒕𝒕𝒑𝒑 ,exactly same as that of the basic CMOS inverter from **Part 0**? If not, what is the percentage deviation from the basic inverter’s avergae propagation delay?

# Part 3: 2-input XNOR gate design, simulation, and analysis (50 points)

1. **Determine the widths (W) of all the transistors** in the design such that the delays are almost same as that of the basic inverter in **Part 0**.

# Include the diagram of the 2-input CMOS XNOR logic clearly indicating the (W/L) of each transistor. Note: the diagram should NOT be hand-drawn.

# Chart, box and whisker chart A' Description automatically generatedChart, box and whisker chart Description automatically generated

2p=6,

n=2,

p=3,

**B**

**B’**

**A’**

# Diagram, schematic Description automatically generated

2p=6,

P4

P3

P2

P1

2n=4,

2n=4,

2n=4,

2n=4,

2p=6,

2p=6,

1. Model the circuit in HSPICE, perform the HSPICE simulation, and note down the following parameters.

|  |  |  |
| --- | --- | --- |
| **Performance Parameters** | **2-input XNOR gate** | |
|  | 15.6, 22.6, 16, 24.5, | 19.675ps |
|  | 25.6, 19.4, 15.6, 22.8 | 20.85ps |
|  | 20.262ps | |
| **Static Power** | 390.9029nW | |
| **Average Power** | 255.84nW | |

**Include the screenshot of the transient response waveform** to observe the inverter operation up to 20ns and the SPICE netist (.sp file).

1. Is the average propagation delay,𝒕𝒕𝒑𝒑 ,exactly same as that of the basic CMOS inverter from **Part 0**? If not, what is the percentage deviation from the basic inverter’s avergae propagation delay?

**Deliverables:**

**One PDF Report with all the designs, .SP files, simulation results, question answers, waveform snippets, and tables. (20 points)**

**CMOS Inverter Part 0**

\* This is the model for a 45-nm CMOS Inverter Part 0\*

.OPTION POST

.include 'W:\Digital Electronics\device\_45\_nm.lib'

.param len= 45nm

.param Wp= 135nm

.param Wn= 90nm

vdd vdd gnd dc 1V

\*FOR TRANSIENT ANALYSIS

\*PULSE (V1 V2 Td Tr Tf PW Period)

V1 Vin gnd PULSE (0 1 0n 0.01n 0.01n 4n 8n)

\* TRANSISTOR CONNECTION

\*UDN Drain Gate Source Sub device\_type Width Length

M2 Vout Vin vdd vdd pmos W= Wp L= len

M1 Vout Vin gnd gnd nmos W= Wn L= len

CL Vout gnd 3f

\* MEASURING DELAY IN TRANSIENT ANALYSIS

.tran 20p 50n

.measure tpLH TRIG V(Vin) VAL=0.5V FALL=1 TARG V(Vout) VAL=0.5V RISE=1

.measure tpHL TRIG V(Vin) VAL=0.5V RISE=2 TARG V(Vout) VAL=0.5V FALL=2

.measure tp PARAM = '(tpLH + tpHL)/2'

.PRINT V(Vout) V(Vin)

.end

Graphical user interface

Description automatically generated

**CMOS 2-input NAND gate Part 1**

\*This is the model for a 45-nm CMOS 2-input NAND gate Part 1 \*

.OPTION POST

.include 'W:\Digital Electronics\device\_45\_nm.lib'

.param len= 45nm

.param Wp= 135nm

.param Wn= 180nm

vdd vdd gnd dc 1V

\*FOR TRANSIENT ANALYSIS

\*PULSE (V1 V2 Td Tr Tf PW Period)

V1 VA gnd PULSE (1 0 0n 0.01n 0.01n 2n 6n)

V2 VB gnd PULSE (1 0 0n 0.01n 0.01n 6n 10n)

\* TRANSISTOR CONNECTION

\*UDN Drain Gate Source Sub device\_type Width Length

MUA VY VA vdd vdd pmos W= Wp L= len

MUB VY VB vdd vdd pmos W= Wp L= len

MDA VY VA P1 P1 nmos W= Wn L= len

MDB P1 VB gnd gnd nmos W= Wn L= len

CL VY gnd 3f

\* MEASURING DELAY IN TRANSIENT ANALYSIS

.tran 20p 50n

.measure tpLH TRIG V(VA) VAL=0.5V FALL=1 TARG V(VY) VAL=0.5V RISE=1

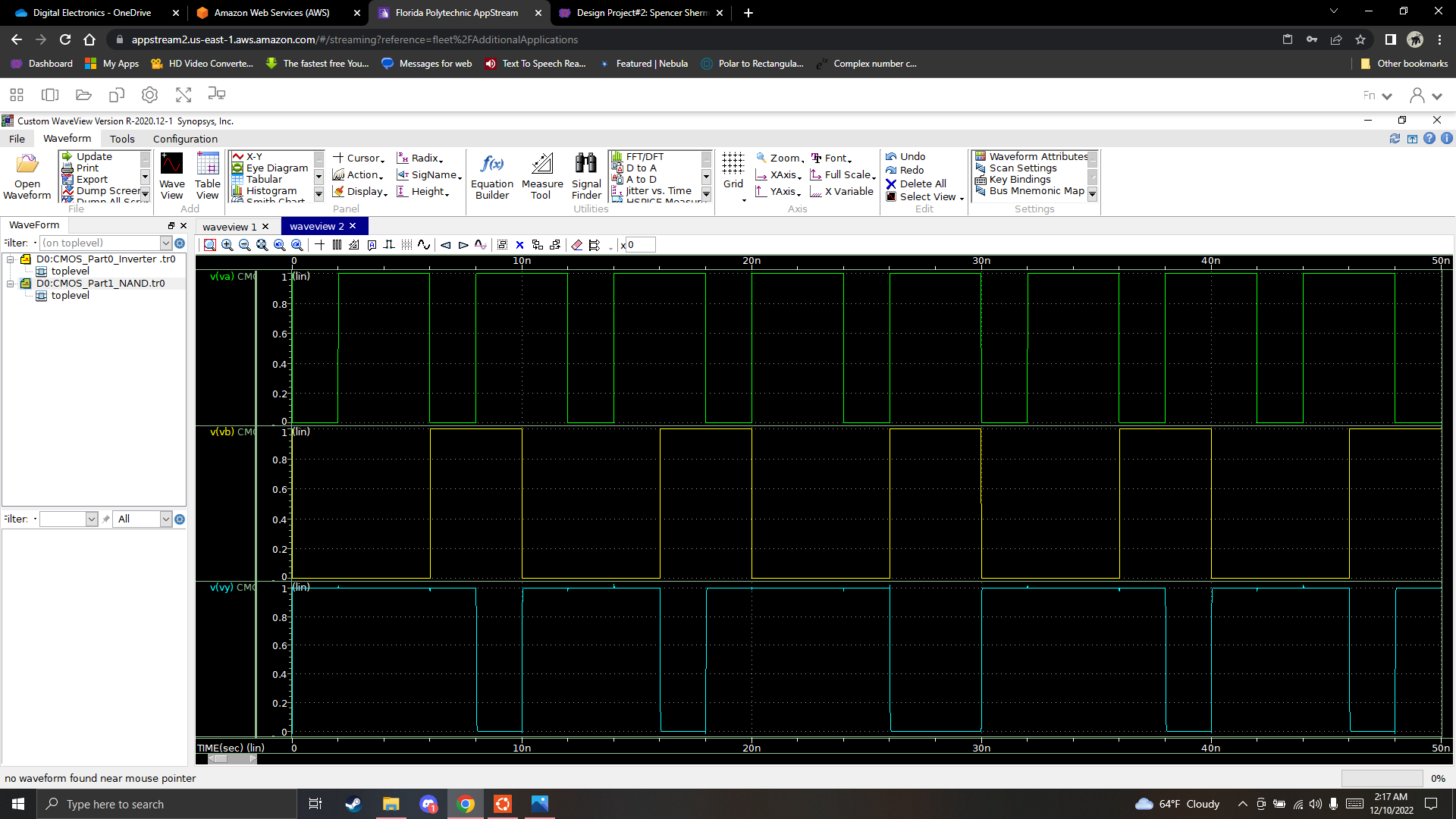
.measure tpHL TRIG V(VA) VAL=0.5V RISE=2 TARG V(VY) VAL=0.5V FALL=2

.measure tp PARAM = '(tpLH + tpHL)/2'

.measure TRAN iavg AVG i(vdd) FROM=18e-9 TO=26e-9

.PRINT V(Vout) V(Vin)

.end



A screenshot of a computer

Description automatically generated

**CMOS 2-input NOR gate part 2**

\* This is the model for a 45-nm CMOS 2-input NOR gate part 2\*

.OPTION POST

.include 'W:\Digital Electronics\device\_45\_nm.lib'

.param len= 45nm

.param Wp= 270nm

.param Wn= 90nm

vdd vdd gnd dc 1V

\*FOR TRANSIENT ANALYSIS

\*PULSE (V1 V2 Td Tr Tf PW Period)

V1 VA gnd PULSE (1 0 0n 0.01n 0.01n 4n 6n)

V2 VB gnd PULSE (1 0 0n 0.01n 0.01n 6n 10n)

\* TRANSISTOR CONNECTION

\*UDN Drain Gate Source Sub device\_type Width Length

MUA P1 VA vdd vdd pmos W= Wp L= len

MUB VY VB P1 P1 pmos W= Wp L= len

MDA VY VA gnd gnd nmos W= Wn L= len

MDB VY VB gnd gnd nmos W= Wn L= len

CL VY gnd 3f

\* MEASURING DELAY IN TRANSIENT ANALYSIS

.tran 20p 50n

.measure tpLH TRIG V(VA) VAL=0.5V FALL=1 TARG V(VY) VAL=0.5V RISE=1

.measure tpHL TRIG V(VA) VAL=0.5V RISE=2 TARG V(VY) VAL=0.5V FALL=2

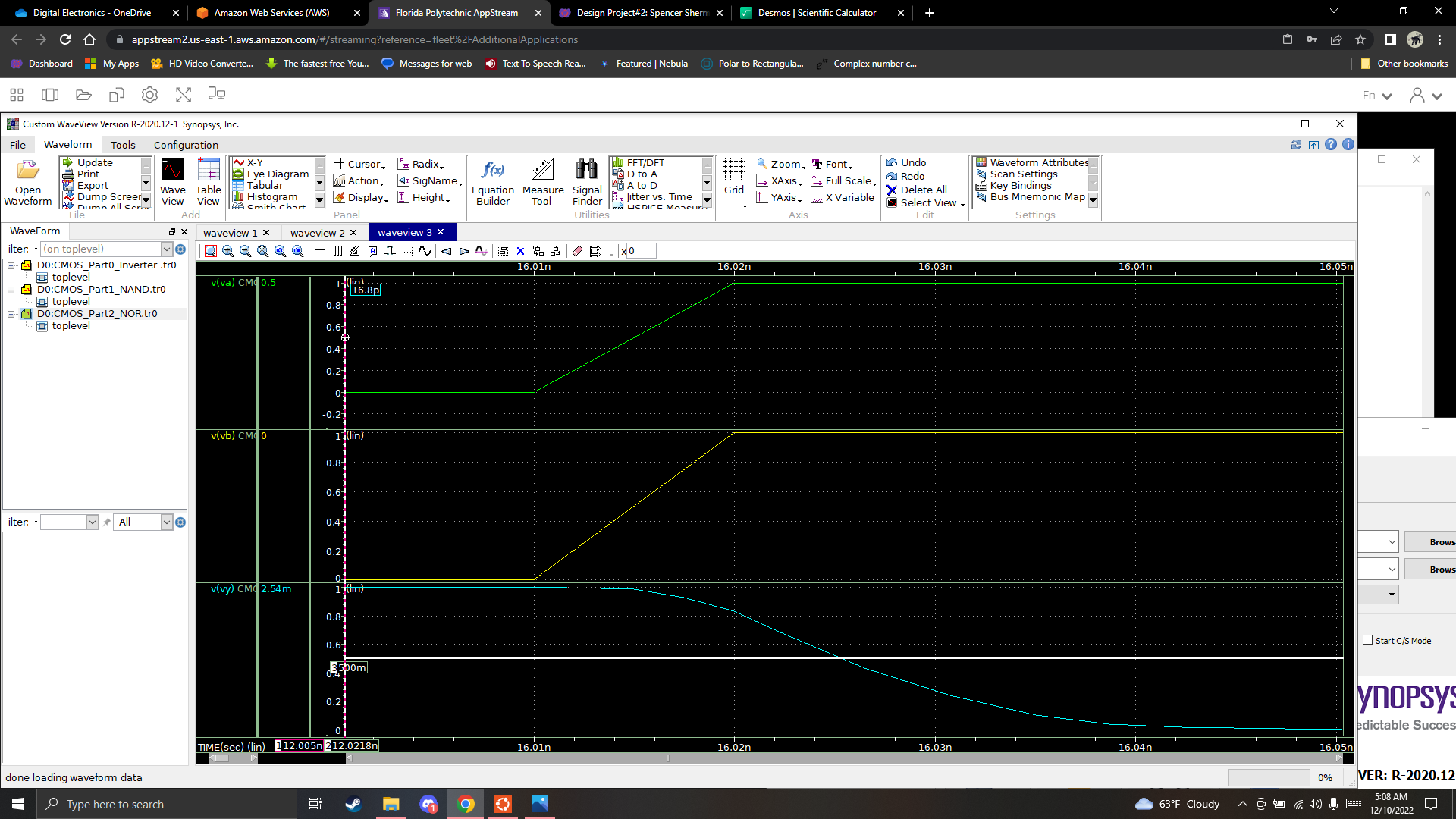
.measure tp PARAM = '(tpLH + tpHL)/2'

.measure TRAN iavg AVG i(vdd) FROM=17e-9 TO=19e-9

.PRINT V(Vout) V(Vin)

.end

A screenshot of a computer

Description automatically generated

**CMOS 2-input XNOR gate part 3**

\* This is the model for a 45-nm CMOS 2-input XNOR gate part 3\*

.OPTION POST

.include 'W:\Digital Electronics\device\_45\_nm.lib'

.param len= 45nm

.param WIp= 135nm

.param WIn= 90nm

.param Wp= 270nm

.param Wn= 180nm

vdd vdd gnd dc 1V

\*FOR TRANSIENT ANALYSIS

\*PULSE (V1 V2 Td Tr Tf PW Period)

V1 VA gnd PULSE (1 0 0n 0.01n 0.01n 2n 4n)

V2 VB gnd PULSE (1 0 0n 0.01n 0.01n 3n 5n)

\* TRANSISTOR CONNECTION

\*UDN Drain Gate Source Sub device\_type Width Length

MIUA VIA VA vdd vdd pmos W= WIp L= len

M1DA VIA VA gnd gnd nmos W= WIn L= len

MIUB VIB VB vdd vdd pmos W= WIp L= len

M1DB VIB VB gnd gnd nmos W= WIn L= len

MUNB P1 VB vdd vdd pmos W= Wp L= len

MUNA VY VA P1 P1 pmos W= Wp L= len

MUIB P2 VIB vdd vdd pmos W= Wp L= len

MUIA VY VIA P2 P2 pmos W= Wp L= len

MDIA VY VIA P3 P3 nmos W= Wn L= len

MDNB P3 VB gnd gnd nmos W= Wn L= len

MDNA VY VA P4 P4 nmos W= Wn L= len

MDIB P4 VIB gnd gnd nmos W= Wn L= len

CL VY gnd 3f

\* MEASURING DELAY IN TRANSIENT ANALYSIS

.tran 20p 50n

.measure tpLH TRIG V(VA) VAL=0.5V FALL=1 TARG V(VY) VAL=0.5V RISE=1

.measure tpHL TRIG V(VA) VAL=0.5V RISE=2 TARG V(VY) VAL=0.5V FALL=2

.measure tp PARAM = '(tpLH + tpHL)/2'

.measure TRAN iavg AVG i(vdd) FROM=13e-9 TO=18e-9

.PRINT V(Vout) V(Vin)

.end

A screenshot of a computer

Description automatically generatedA screenshot of a computer

Description automatically generated